What is Claimed is:

1. A fabricating system comprising:

at least two processing apparatuses, and

an inter-apparatus transporter for transporting works to a desired processing apparatus,

wherein in a period of time when a first group of works are processed or stocked, said inter-apparatus transports remaining groups of works; and

in a period of time when part of said remaining groups of works are processed or stocked, said inter-apparatus transports said first group of works.

2. A fabricating system comprising:

at least two processing apparatuses;

L sets (L; positive integer) of inter-apparatus transporters, each of which is adapted to transport works to a desired processing apparatus; and

a loading and unloading apparatus for loading and unloading works to and from said fabricating system,

wherein said processing apparatus includes;

a means for receiving a set of works (M pieces, M: positive integer) from either of said inter-apparatus transporters for a time interval T min (T: positive number) after a time To;

a means for stocking said works;

a means for applying a sequence of processes to a set of works received before the time To;

a means for unloading a set of already-processed works to either of said inter-apparatus transporters at a time (To+N×T, N: positive integer), and

each of said inter-apparatus transporters directly transports works, between at least two processing apparatuses capable of applying a continued process to works, for a time interval L×T min or less, and which has a means for transporting a set of works, said works being started to be unloaded from a processing apparatus at a time (To+N×T), to another processing apparatus capable of applying a continued process to works, until a time (To+(N+L)×T).

3. A fabricating system comprising:

L sets of inter-apparatus transporters capable of transporting a set of works (M pieces), between processing apparatuses capable of applying a continued process to works, for a time interval less than (L×T) min;

an apparatus connected to each of said inter-apparatus transporters for loading and unloading works to and from said fabricating system; and

at least two processing apparatuses connected to said inter-apparatus transporters each of which, in a period of time from To to (To+T), receives a first set of works, starts to process a second set of works received for a time interval from (To-T) to To, and unloads a third set of works which are already processed for a time interval from (To-T) to To, to said inter-apparatus transporters.

4. A fabricating system according to claim 2, wherein

said work is a semiconductor wafer, and

said processing apparatus is a semiconductor processing apparatus for applying either of a cleaning process, CVD film deposition process, a film formation process including sputter film deposition or coating film formation, heat-treatment process including diffusion, oxidization or nitrization, exposing process by an energy particle beam such as a light beam, electron beam or X-ray, resist process including coating, development or baking, etching process including dry etching or wet etching, impurities introducing process by ion implantation or the like, resist removing process by ashing or the like, planarization process including chemical mechanical polishing, and detecting process.

5. A fabricating system according to claim 4, wherein said semiconductor processing apparatus includes a first

stocking means for receiving a set of semiconductor wafers from said inter-apparatus transporter, and a second stocking means for unloading a set of semiconductor wafers to said inter-apparatus.

6. A fabricating system according to claim 4, wherein said semiconductor apparatus includes a first stocking means connected to said inter-apparatus transporter for receiving and stocking at least one set of semiconductor wafers; a first preparing chamber provided adjacently to said first stocking means; a transporting chamber provided adjacently to said first preparing chamber; a second preparing chamber provided adjacently to said transporting chamber; and a second stocking means provided adjacently to said second preparing chamber for stocking and unloading at least one set of semiconductor wafers.

7. A fabricating system according to claim 5, wherein

said semiconductor processing apparatus is a metal film deposition apparatus; and

said metal film deposition apparatus includes a first preparing chamber provided adjacently to said first stocking means; a transporting chamber provided adjacently to said first preparing chamber; a pre-treatment chamber and a metal film deposition chamber provided adjacently to said transporting chamber; and a second preparing chamber

provided adjacently to said transporting chamber and said second stocking means.

8. A fabricating system according to claim 5, wherein

said semiconductor processing apparatus is an insulator film deposition apparatus; and

said insulator film deposition apparatus includes a first preparing chamber provided adjacently to said first stocking means; a transporting chamber provided adjacently to said first preparing chamber; an insulator film deposition chamber provided adjacently to said transporting chamber; and a second preparing chamber provided adjacently to said transporting chamber and said second stocking means.

9. A fabricating system according to claim 5, wherein

said semiconductor processing apparatus is a dry etching apparatus; and

said dry etching apparatus includes a first preparing chamber provided adjacently to said first stocking means; a transporting chamber provided adjacently to said first preparing chamber; a dry etching and ashing chamber provided adjacently to said transporting chamber; and a second preparing chamber provided adjacently to said transporting chamber and said second stocking means.

10. A fabricating system according to claim 5, wherein

said semiconductor processing apparatus is a lithography apparatus; and

said lithography apparatus includes a coating chamber provided adjacently to said first stocking means; a baking chamber provided adjacently to said coating chamber; an exposing chamber provided adjacently to said baking chamber; and a developing chamber provided adjacently to said exposing chamber and said second stocking means.

11. A fabricating system according to claim 5, wherein the stay period of said semiconductor wafers in said stocking means is within a time interval T min inherent in said fabricating system.

12. A fabricating system according to claim 5, wherein said semiconductor processing apparatus further includes a first preparing chamber provided adjacently to said first stocking means; a transporting chamber provided adjacently to said first preparing chamber; processing chambers (Q pieces, Q: positive integer) provided adjacently to said transporting chamber, the processing time in said processing chambers being $(Q-1)\times T$ min or more and less than $Q\times T$ min; and a second preparing chamber

provided adjacently to said second stocking means which is provided adjacently to said transporting chamber.

13. A fabricating system according to claim 5, wherein said fabricating system, as said semiconductor processing apparatus, includes a metal film deposition apparatus, an insulator film deposition apparatus, a lithography apparatus, a metal film dry etching apparatus, and an insulator film dry etching apparatus.

14. A fabricating system according to claim 5, wherein each of said first and second stocking means has a stocking means for stocking at least one set of semiconductor wafers to be simultaneously processed in said semiconductor processing apparatuses.

15. A fabricating system according to claim 5, wherein said fabricating system further includes a stocking apparatus connected to said inter-apparatus transporters of L pieces for containing at least one set of semiconductor wafers impossible to be simultaneously processed, other than said first and second stocking means provided in said semiconductor processing apparatus.

16. A fabricating system according to claim 15, wherein

said stocking apparatus receives and stocks at least one set of semiconductor wafers from said transporters of L

pieces for a time interval L×T min after the time To; unloads a set of semiconductor wafers received before the time To to either of said inter-apparatus transporters at a time (To+ L×T); and which is connected to all of processing apparatuses to be unloaded from said stocking apparatus, by means of said inter-apparatus transporters capable of directly transporting semiconductor wafers between processing apparatuses for a time interval of less than L×T min; and

each of said inter-apparatus transporters has a means for transporting, until a time (To+(N+L)×T), a set of semiconductor wafers started to be unloaded from said stocking apparatus at the time (To+ N×T), to a processing apparatus capable of applying a continued process to semiconductor wafers, or transporting, until a time (To+(N+L)×T), a set of semiconductor wafers started to be unloaded from said processing apparatus at the time (To+ N×T), to said stocking apparatus.

17. A fabricating system according to claim 4, wherein

an inter-apparatus for transporting semiconductor wafers between at least two processing apparatuses capable of applying a continued process to semiconductor wafers,

among said transporters, is of a single wafer transporting type for transporting semiconductor wafers one by one.

18. A fabricating system according to claim 4, wherein each of at least two processing apparatuses capable of applying a continued process to semiconductor wafers, among said processing apparatuses, is a single wafer processing type for processing said semiconductor wafers one by one.

19. A fabricating system according to claim 17, wherein said semiconductor wafer is continuously subjected to all of a sequence of predetermined processes.

20. A fabricating system according to claim 19, wherein said processing apparatus for applying a continued process to said semiconductor wafer is a lithography apparatus for continuously applying, to said semiconductor wafers, a sequence of lithography processes including exposing by an energy particle beam and resist processing.

21. A fabricating system according to claim 20, wherein said processing apparatus for applying a continued process to said semiconductor wafers further includes a second processing apparatus for applying, to said semiconductor wafers, a process which is continued to and not included in said lithography process.

22. A fabricating system according to claim 21, wherein said second processing apparatus is an etching apparatus.

23. A fabricating system according to claim 21, said second processing apparatus is an impurities introducing apparatus.

24. A fabricating system according to claim 19, wherein said processing apparatus for applying a continued process to said semiconductor wafers includes a second processing apparatus for continuously applying, to said semiconductor wafers, a sequence of resist removing processes including resist removing and cleaning.

25. A fabricating system according to claim 24, wherein said processing apparatus for applying a continued process to said semiconductor wafers includes a third processing apparatus for applying a process not included in said resist removing processes to said semiconductor wafers before said resist removing processes, and a fourth processing apparatus for applying, to said semiconductor wafers, the first process of a sequence of said resist removing processes.

26. A fabricating system according to claim 25, wherein said third processing apparatus is an etching apparatus.

27. A fabricating system according to claim 25, wherein said third processing apparatus is an impurities introducing apparatus.

28. A fabricating system according to claim 19, wherein said processing apparatus for applying a continued process to said semiconductor wafers includes a processing apparatus for applying, to said semiconductor wafers, metallization processes including steps of depositing at least one layer of a metal film and an interlayer insulator film,

said metallization processes including a film formation process including CVD film deposition, sputter film deposition or coating film formation, an exposing process by an energy particle beam, a resist process including coating, developing, baking and resist removing, an etching process, and a resist removing process.

29. A fabricating system according to claim 4, wherein

each of L piece of said inter-apparatus transporters is looped, and

said fabricating system includes an apparatus connected to said inter-apparatus transporters for loading and unloading semiconductor wafers, and at least two

processing apparatuses connected to said inter-apparatus transporters.

30. A fabricating system according to claim 29, wherein each of said looped inter-apparatus transporters has a means for transporting said works for one round along one direction for a time interval of less than L×T min.

31. A fabricating system according to claim 30, wherein each of said inter-apparatus transporters transports said works while being repeatedly moved or stopped, and has a means for loading and unloading said works between said inter-apparatus transporter and said processing apparatus at the time of stoppage.

32. A fabricating system according to claim 4, L is 1.

33. A fabricating system according to claim 4, M is 1.

34. A fabricating system according to claim 4, N is 1.

35. A fabricating system according to claim 4, T is in the range of $0<T\leqq10$.

36. A fabricating system according to claim 4, wherein T is in the range of $0<T\leqq7$.

37. A fabricating system according to claim 4, wherein T is in the range of $0<T\leqq5$.

38. A fabricating system according to claim 4, wherein T is in the range of $0<T\leqq 3$.

39. A fabricating system according to claim 4, wherein said semiconductor processing apparatus has a means for identifying the kind of said semiconductor wafer.

40. A fabricating system according to claim 4, wherein each processing chamber provided in said semiconductor processing apparatus has a means for identifying the kind of semiconductor wafer.

41. A fabrication system according to claim 39, wherein the output from said identifying means is used as an interlock starting signal for preventing a process from being applied to semiconductor wafers not to be processed or preventing a process from being applied to semiconductor wafers under an erroneous condition.

42. A fabricating system according to claim 4, wherein said processing apparatus is disposed on one side of said inter-apparatus transporter for enabling maintenance and checking to be performed from the side opposed to said inter-apparatus transporter.

43. A fabricating system according to claim 4, wherein at least one of said processing apparatuses for applying the exposing process by an energy particle beam is

disposed substantially at the center of said fabricating system.

44. A fabricating system according to claim 4, wherein at least one of said processing apparatuses for applying the cleaning process is disposed substantially at the center of said fabricating system.

45. A fabricating system according to claim 4, wherein at least one of said processing apparatus for applying the oxidizing or nitrizing process is disposed substantially at the center of said fabricating system.

46. A fabricating system according to claim 17, wherein said inter-apparatus single wafer transporter has a means for transporting semiconductor wafers through an atmosphere controlled independently from the surroundings of said single wafer transporter, said atmosphere includes a gas mainly containing nitrogen, vacuum or an air with a high cleanliness.

47. A fabricating system according to claim 46, wherein said inter-apparatus single wafer transporter has a means for detecting said semiconductor wafers.

48. A fabricating system according to claim 47, wherein said inter-apparatus single wafer transporter has a means for controlling the environmental condition of a

transporting passage such as a flow of gas on the basis of said detecting means.

49. A fabricating system according to claim 46, wherein said inter-apparatus single wafer transporter has a means for making the flow of gas in said transporting passage into a substantially laminar flow.

50. A fabricating system according to claim 15, wherein said stocking apparatus is capable of containing all of said semiconductor wafers in said fabricating system.

51. A fabricating system according to claim 4, which further comprises:

at least one of a preliminary processing chamber and an inter-apparatus single wafer transporting unit, which is disposed in the same environment as the environment in which said processing apparatuses and said inter-apparatus single wafer transporters are disposed; and

an exchange means for easily performing the exchange of said preliminary processing apparatus or said inter-apparatus single wafer transporting unit.

52. A fabricating system according to claim 4, which previously includes, at least one spare processing apparatus or common processing apparatus capable of

applying the same process, for at least one of said processing apparatuses.

53. A fabricating method comprising the steps of:

processing works by at least two processing apparatuses; and

transporting works by an inter-apparatus transporter capable of transporting works to a desired processing apparatus;

wherein in a period of time when a first group of works are processed or stocked, remaining groups of works are transported or stocked, and

in a period of time when said first group of works are transported or stocked after being processed, one group of works of said remaining groups of works are processed or stocked.

54. A fabricating method including the steps of: applying at least two continued processes to a plurality of sets of works (M pieces, M: positive integer); and transporting works by L sets (L: positive integer) of inter-apparatus transporters capable of transporting works to a desired processing apparatus, said method comprising the steps of:

loading and stocking a set of works from either of said inter-apparatus transporters to at least one

processing apparatus or to at least one of a plurality of processing apparatuses having the same processing function for a time interval T min (T: positive number) after To;

processing one set of works loaded before a time To in said processing apparatus;

unloading a set of the works already processed from said processing apparatus to either of said inter-apparatus transporter at a time (To+N×T) (N: positive integer); and

transporting a set of works started to be unloaded from a processing apparatus at the time (To+N×T) to another processing apparatus until a time (To+(N+L)×T).

55. A fabricating method according to claim 54, wherein a set of works already processed started to be unloaded from at least one of said processing apparatuses or from at least one of a plurality of processing apparatuses having the same function to said inter-apparatus transporter at the time (To+N×T) are those processed for a time interval T min from a time (To+(N-1)×T) to (To+N×T).

56. A fabricating method comprising the steps of:

loading a set of works (M pieces) to an loading/unloading apparatus at a time To, said loading and unloading apparatus being connected to L pieces of inter-apparatus transporters capable of transporting a set of

works (M pieces) between processing apparatuses for a time interval less than L×T min;

transporting a set of said works to a first processing apparatus, of at least two processing apparatuses connected to said transporters, by said transporters for a time interval from the time To to (To+ L×T); and

starting to process a second set of works already loaded in said first processing apparatus for a time interval from (To-T) to To; unloading a third set of works already processed in said first processing apparatus to said inter-apparatus transporters for a time interval from the time (To-T) to To; and transporting a fourth set of works unloaded from said first processing apparatus to said inter-apparatus transporters to a second processing apparatus different from said first processing apparatus for a time interval from the time (To-T) to a time (To+(L-1))×T.

57. A fabricating method according to claim 54,

wherein said work is a semiconductor wafer; and

said process is either of processes applied to a semiconductor wafer in the LSI fabrication including a cleaning process; a film formation process including CVD film deposition, sputter film deposition or coating film formation; heat-treatment process including diffusion,

oxidization and nitrization; exposing process by an energy particle beam such as a light beam, electron beam or X-ray; a resist process including coating, developing and baking; etching process including dry etching and wet etching; impurities introducing process such as ion implantation; a resist removing process by ashing or the like; planarization process including chemical or mechanical grinding; detection process including length measurement or foreign matter detection.

58. A fabricating method according to claim 57, which further comprises the step of containing at least one set of semiconductor wafers impossible to be simultaneously processed in a semiconductor wafer stocking mechanism provided in each of said processing apparatus.

59. A fabricating method according to claim 57, which further comprises the step of containing at least one set of semiconductor wafers impossible to be simultaneously processed in a stocking apparatus connected to said inter-apparatus transporters, different from said semiconductor wafer stocking mechanism provided in each of said processing apparatus.

60. A fabrication method according to claim 59, which further comprises the step of:

loading at least one set of semiconductor wafers from either of said inter-apparatus transporters to said stocking apparatus for a time interval (L×T) min after a time To;

unloading a set of semiconductor wafers loaded before the time To from said stocking apparatus to either of said inter-apparatus transporters at a time (To+N×T); and

transporting, until a time (To+(N+L)×T), a set of semiconductor wafers started to be unloaded from said stocking apparatus at the time (To+N×T) to a processing apparatus, or transporting a set of semiconductor wafers started to be unloaded from a processing apparatus to said stocking apparatus.

61. A fabricating method according to claim 57, which further comprises the step of applying continued processes to a plurality of sets of semiconductor wafers at a basis cycle of T min after a time To,

wherein T is the maximum value or more of (the minimum time intervals required to unload semiconductor wafers already processed to said inter-apparatus transporter), in a group of processing apparatuses for applying continued processes to sets of semiconductor wafers.

62. A fabricating method according to claim 57, which further comprises the step of applying continued processes

to a plurality of sets of semiconductor wafers at a basis cycle of T min after a time To,

wherein T is the maximum value or more of (the minimum time intervals required to unload sets of semiconductor wafers to said inter-apparatus transporters/the number of processing apparatuses having the same function), in a group of processing apparatuses for applying continued processes to sets of semiconductor wafers.

63. A fabricating method according to claim 57, which comprising the step of:

applying a process requiring a processing time of (Q-1)×T min and less than Q×T min to a set of semiconductor wafers using a processing apparatus composed of Q pieces of processing units having the same function,

wherein the timing of processing performed in each apparatus of said processing apparatus is shifted for applying a process to a plurality of sets of semiconductor wafers at a basic cycle T min after the time To; and

said processing apparatus receives and stocks at least one set of semiconductor wafers from said inter-apparatus transporter at a cycle T min, processing a set of semiconductor wafers received before the time To, and unloads a set of semiconductor already processed to said inter-apparatus transporters at a time (To+N×T).

64. A fabricating method according to claim 57, which further comprises the step of applying a continued process to a set of semiconductor wafers at a basic cycle of T min after the time To,

wherein when sets of semiconductor wafers are of one kind, T is the minimum time value or more required to unload to said transporters a set of semiconductor wafers processed in such a processing apparatus as to be maximized in the value of (the minimum time interval required to unload a set of already-processed semiconductor wafers to said transporters×the processing number of each set of semiconductor wafers); and

when sets of semiconductor wafers are of a plurality of kinds, T is the minimum time value or more required to unload to said transporters a set of semiconductor wafers processed in such a processing apparatus as to be maximized in the value of (the minimum time interval required to unload a set of already-processed semiconductor wafers to said transporters×the weighted mean of the processing number of each set of semiconductor wafers).

65. A fabricating method according to claim 57, which further comprises a step of continuously processing a plurality of semiconductor wafers with a basic cycle T min based on a certain time To;

wherein when sets of semiconductor wafers are of one kind, T is the minimum time interval or more required to unload to said transporters a set of semiconductor wafers processed in such a processing apparatus as to be maximized in the value of (the minimum time interval required to unload a set of already-processed semiconductor wafers to said transporter×the processing number of each set of the semiconductor wafers/the number of processing apparatuses having the same function); and

when sets of semiconductor wafers are of a plurality of kinds, T is the minimum time interval or more required to unload to said transporter a set of semiconductor wafers processed in such a processing apparatus as to be maximized in the value of (the minimum time interval required to unload a set of already-processed semiconductor wafers to said transporter×the weighted mean of the processing number of each set of semiconductor wafers/the number of the processing apparatuses having the same function).

66. A fabricating method according to claim 57, wherein when the maximum transporting time between two processing apparatuses by L pieces of said transporters is (R-1)×T min or more and less than R×T min (R: positive integer), R is taken as L, and

a plurality of sets of semiconductor wafers are continuously processed at a basic cycle of T min after a time To.

67. A fabricating method according to claim 57, which further comprising the steps of unloading a group of semiconductor wafers in the number equivalent to L/(L+1) of semiconductor wafers in the processing stage and transporting or stocking to or in another processing apparatus capable of applying continued a process to semiconductor wafers, in a time interval L×T min after a certain time To, and

processing a group of semiconductor wafers possible to be processed among the remaining groups of semiconductor wafers in each processing apparatus, similarly in a time interval L×T min after a certain time To.

68. A fabricating method according to claim 57, which further comprising the steps of:

applying the m-th process to the n-th set of said semiconductor wafers (n, m: positive integer) for a time interval from (n+2×m-3)×T min to (n+2×m-2)×T min based on a certain time To,

performing the transporting from a processing apparatus where the m-th process is performed to a processing apparatus where the (m+1)-th process is

performed for a time interval from (n+2×m-2)×T min to (n+2×m-1+L)×T min, and

applying the (m+1)-th process to the n-th set of said semiconductor wafers for a time interval from (n+2×m-1+L)×T min to (n+2×m+L)×T min.

69. A fabricating method according to claim 57, which further comprising the step of;

determining the scheduling for processing and inter-apparatus transporting prior to said processing; and

performing said processing on the basis of said scheduling.

70. A fabricating method according to claim 69, which further comprising the steps of:

determining the scheduling for processing and inter-apparatus transporting prior to said processing, and performing said processing on the basis of said scheduling;

wherein said scheduling is determined on the basis of the step of:

applying the m-th process to the n-th set of said semiconductor wafers (n, m: positive integer) for a time interval from (n+2×m-3)×T min to (n+2×m-2)×T min based on a certain time To,

performing the transporting from a processing apparatus where the m-th process is performed to a

processing apparatus where the (m+1)-th process is performed for a time interval from (n+2×m-2)×T min to (n+2×m-1+L)×T min, and

applying the (m+1)-th process to the n-th set of said semiconductor wafers for a time interval from (n+2×m-1+L)×T min to (n+2×m+L)×T min.

71. A fabricating method according to claim 57, which further comprises the step of:

applying continued processes to a plurality of semiconductor wafers at a basic cycle T min based on a certain time To while adjusting the presence or absence of the loading of a set of semiconductor wafers for each time interval T min,

wherein when sets of semiconductor wafers are of one kind, an average loading time interval is the maximum value or more of (T (min)×the processing number of each set of semiconductor wafers) of a group of processing apparatuses for applying continued processes to sets of semiconductor wafers; and

when sets of semiconductor wafers are a plurality of kinds, said average loading time interval is the maximum value of (T (min)×the weighted mean of the processing number of each set of semiconductor wafers) of a group of said processing apparatuses.

72. A fabricating method according to claim 57, which further comprises the step of:

applying continued processes to a plurality of semiconductor wafers at a basic cycle T min based on a certain time To while adjusting the presence or absence of the loading of a set of semiconductor wafers for each time interval T min,

wherein when sets of semiconductor wafers are of one kind, an average loading time interval is the maximum value or more of (T (min)×the processing number of each set of semiconductor wafers/the number of processing apparatuses having the same function) of a group of processing apparatuses for applying continued processes to sets of semiconductor wafers; and

when sets of semiconductor wafers are a plurality of kinds, said average loading time interval is the maximum value of (T (min)×the weighted mean of the processing number of each set of semiconductor wafers/the number of processing apparatuses having the same function) of a group of said processing apparatuses.

73. A fabricating method according to claim 57, wherein said step for applying continued processes comprises the step of applying a sequence of lithography processes including exposure by an energy particle beam

such as a light beam, electron beam or X-ray, and resist processing including coating, developing and baking.

74. A fabricating method according to claim 57, wherein said step for applying continued processes comprises the step of applying the last process in a sequence of lithography processes including exposure by an energy particle beam such as a light beam, electron beam or X-ray, and resist processing including coating, developing and baking, and the step of applying a process which is continued to and not contained in said lithography processes.

75. A fabricating method according to claim 74, wherein said step which is continued to and not contained in said lithography processes comprises the step of applying an etching process such as dry etching or wet etching.

76. A fabricating method according to claim 74, wherein said step which is continued to and not contained in said lithography processes comprises the step of applying an impurities introducing process by ion implantation or the like.

77. A fabricating method according to claim 57, wherein said step of applying continued processes comprises the step of applying a sequence of resist removing

processes including resist removing by ashing or the like and cleaning.

78. A fabricating method according to claim 57, wherein said step of applying continued processes comprises the step of applying a process not contained in a sequence of resist removing processes including resist removing by ashing and cleaning, prior to a sequence of said resist removing processes; and the step of applying the first process of a sequence of resist removing processes.

79. A fabricating method according to claim 78, wherein said step of applying a process not contained in said resist removing processes prior to a sequence of said resist removing processes comprises the step of applying an etching process including dry etching or wet etching.

80. A fabricating method according to claim 78, wherein said step of applying a process not contained in said resist removing processes prior to a sequence of said resist removing processes comprises the step of applying an impurities introducing process by ion implantation or the like.

81. A fabricating method according to claim 57, wherein said step of applying continued processes comprises all of the steps of applying metallization processes for depositing at least one layer of a metal film and an

interlayer insulator film, said metallization processes comprising a film formation process including CVD film deposition, sputter film deposition or coating film formation; exposing process by an energy particle beam such as a light beam, electron beam or X-ray; resist process including coating, developing, baking or resist removing; etching process including dry etching or wet etching; and a resist removing process by ashing or the like.

82. A fabricating method according to claim 57, wherein L is 1.

83. A fabricating method according to claim 57, wherein M is 1.

84. A fabricating method according to claim 57, wherein N is 1.

85. A fabricating method according to claim 57, wherein T is in the range of $0<T\leqq10$.

86. A fabricating method according to claim 57, wherein T is in the range of $0<T\leqq7$.

87. A fabricating method according to claim 57, wherein T is in the range of $0<T\leqq5$.

88. A fabricating method according to claim 57, wherein T is in the range of $0<T\leqq3$.

89. A fabricating system including at least two processing apparatuses and an inter-apparatus transporter

capable of transporting semiconductor wafers to a desired processing apparatus, comprising a means for managing the managing information of process progress and the scheduling information of processing and transporting for semiconductor wafers contained in said system.

90. A fabricating system according to claim 89, which further comprises a means for preparing said scheduling information of processing and transporting.

91. A fabricating system according to claim 89, which further comprises a means for comparing said managing information of process progress and said scheduling information of processing and transporting for semiconductor wafers with each other.

92. A fabricating system according to claim 91, which further comprises a means for determining at least part of the operational conditions of said processing apparatuses or said inter-apparatus transporter on the basis of the result of comparing said managing information of process progress and said scheduling information of processing and transporting for semiconductor wafers with each other.

93. A fabricating system according to claim 92, which further comprises a means of renewing said scheduling information of processing and transporting on the basis of the result of comparing said managing information of

process progress and said scheduling information of processing and transporting for semiconductor wafers with each other.

94. A fabricating system according to claim 89, said managing information of process progress or said scheduling information of processing and transporting for said semiconductor wafers is for each semiconductor wafer.

95. A fabricating system according to claim 89, which further comprises a means of managing the information on result of processing and transporting for said semiconductor wafers.

96. A fabricating system according to claim 95, which further comprises a means of determining at least part of the operational conditions of said processing apparatuses or said inter-apparatus transporter on the basis of said information on result of processing and transporting for said semiconductor wafers.

97. A fabricating system according to claim 96, said information on result of processing and transporting is for each semiconductor wafer.

98. A fabricating system according to claim 89, which further comprises a plurality of data bases containing the managing information of process progress of at least part of said semiconductor wafers.

99. A fabricating system according to claim 89, which further comprises a plurality of data bases containing the scheduling information of processing and transporting of at least part of said semiconductor wafers.

100. A fabricating system according to claim 89, which further comprises a plurality of data bases containing the information on result of processing and transporting of at least part of said semiconductor wafers.

101. A fabricating system according to claim 98, wherein computers each having a function of controlling processing and transporting operations and a function of managing at least one of said data bases are distributed in each or a set of processing apparatuses and inter-apparatus transporters.

102. A fabricating system according to claim 101, wherein each of said computers manages at least one of said data bases on semiconductor wafers contained in each or a set of said processing apparatuses and said inter-apparatus transporters.

103. A fabricating system according to claim 98, wherein computers, each having a function of controlling processing and transporting operations and a function of transmitting a data for renewing at least one of said data bases to each of said computers having a function of

managing at least one of said data bases, are distributed in each or a set of said processing apparatuses and said inter-apparatus transporters.

104. A fabricating system according to claim 103, said computers, which are distributed in each or a set of said processing apparatus and said transporters, transmit a data for renewing the data base, to said computers for managing at least one of the data bases containing said managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting on semiconductor wafers contained in each or a set of said processing apparatuses and said inter-apparatus transporters.

105. A fabricating system according to claim 103, wherein said computers distributed in each or a set of said processing apparatus and said transporters, each of which has a function of receiving said managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting on semiconductor wafers contained in each or a set of processing apparatuses and said inter-apparatus transporters, from computers distributed in each or a set of different processing apparatuses and inter-apparatus

transporters from said processing apparatuses and said inter-apparatus transporters.

106. A fabricating system according to claim 104, wherein when semiconductor wafers in said fabricating system are moved between each or a set of processing apparatuses and inter-apparatus transporters, said managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting on said semiconductor wafers are moved between said computers by transmission or receiving of the managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting between said computers.

107. A fabricating system according to claim 101, at least two of said computers distributed in said processing apparatuses and said inter-apparatus transporters are connected to the same data field in said system.

108. A fabricating system according to claim 107, wherein said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters have a function of transmitting a data with a content identification element attached to said data field, and

at least one of computers distributed in each or a set of different processing apparatuses and inter-apparatus transporters from said processing apparatuses and said inter-apparatus transporters has a function of receiving a data identified and selected by said content identification element from said data field.

109. A fabricating system according to claim 107, wherein said data field is a memory such as a main line of a local area network, semiconductor memory and a magnetic disk.

110. A fabricating system according to claim 89, which includes a computer having a function of generally managing the managing information of process progress and scheduling information of processing and transporting on all of said semiconductor wafers.

111. A fabricating system according to claim 110, which includes a computer having a function of generally managing the information on result of processing and transporting on all of said semiconductor wafers.

112. A fabricating system according to claim 107, wherein said computer having a function of generally managing said information on all of said semiconductor wafers is connected to the same data field in said system.

113. A fabrication system according to claim 110, wherein said computer having a function of generally managing said information on all of said semiconductor wafers has a function of generally determining at least part of the operational conditions or scheduling of processing or transporting on all of semiconductor wafers contained in said system, on the basis of the result of comparing said managing information of process progress and the scheduling information of processing and transporting on said semiconductor wafers with each other, or on the basis of the information on result of processing and transporting.

114. A fabricating system according to claim 110, which further includes a processing and transporting managing system capable of applying continued processes to a plurality of semiconductor wafers, on the basis of the scheduling information of processing and transporting generally managed by said computer having a function of generally managing said information on said semiconductor wafers.

115. A fabricating system according to claim 113, which further includes a processing and transporting managing system capable of applying continued processes to a plurality of semiconductor wafers, on the basis of the

scheduling of processing and transporting generally determined by said computer having a function of generally managing said information on said semiconductor wafers.

116. A fabricating system according to claim 107, which further includes a processing and transporting managing system capable of applying continued processes to a plurality of semiconductor wafers, on the basis of the scheduling of processing and transporting generally determined by said computers distributed in each or a set of processing apparatuses and said inter-apparatus transporters.

117. A fabricating system according to claim 115, which further includes a plurality of means capable of determining the scheduling of processing and transporting, and an apparatus capable of displaying either of a plurality of said means in which the scheduling of processing and transporting is determined.

118. A fabricating system according to claim 89, which has a function of reading or writing the managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting which are contained in a semiconductor wafer.

119. A fabricating system according to claim 118, which has a function of renewing said information contained in said semiconductor wafer in the processing, transporting or stocking stages.

120. A fabricating system according to claim 118, said semiconductor wafer has the information on result of processing reflected by the result of processing for each semiconductor wafer.

121. A fabricating system according to claim 89, said inter-apparatus transporter is of an inter-apparatus single wafer transporting type.

122. A fabricating system according to claim 89, said processing apparatus is of a single wafer processing type.

123. A fabricating method comprising the steps of:

processing semiconductor wafers by at least two processing apparatuses; and

transporting semiconductor wafers by an inter-apparatus transporter,

wherein the managing information of process progress and scheduling information of processing and transporting on semiconductor wafers contained in said fabricating system are managed by computers contained in said fabricating system.

124. A fabricating method according to claim 123, which further comprises the step of preparing said scheduling information of processing and transporting by said computers contained in said fabricating system.

125. A fabricating method according to claim 123, which further comprises the step of comparing the managing information of process progress and scheduling information of processing and transporting with each other by said computers contained in said fabricating system.

126. A fabricating method according to claim 125, which further comprises the step of determining at least part of the operational conditions of processing apparatuses and inter-apparatus transporter, on the basis of the result of comparing the managing information of process progress and scheduling information of processing and transporting with each other by said computers contained in said fabricating system.

127. A fabricating method according to claim 126, which further comprises the step of renewing said scheduling information of processing and transporting, on the basis of the result of comparing the managing information of process progress and scheduling information of processing and transporting with each other by said computers contained in said fabricating system.

128. A fabricating method according to claim 123, wherein said managing information of process progress or scheduling information of processing and transporting on said semiconductor wafers is for each semiconductor wafer.

129. A fabricating method according to claim 123, which further comprises the step of managing said information on result of processing and transporting on said semiconductor wafers contained in said system by said computers contained in said fabricating system.

130. A fabricating method according to claim 129, which further comprises the step of determining at least part of the operational conditions of processing apparatuses and inter-apparatus transporter, on the basis of the information on result of processing and transporting on said semiconductor wafers by said computers contained in said fabricating system.

131. A fabricating method according to claim 130, wherein the information on result of processing and transporting on said semiconductor wafers is for each semiconductor wafer.

132. A fabricating method according to claim 123, which further comprises the step of containing, the managing information of process progress on at least part

of semiconductor wafers contained in said fabricating system, in a plurality of said data bases.

133. A fabricating method according to claim 123, which further comprises the step of containing, the scheduling information of processing and transporting on at least part of semiconductor wafers contained in said fabricating system, in a plurality of said data bases.

134. A fabricating method according to claim 123, which further comprises the step of containing, the information on result of processing and transporting on at least part of semiconductor wafers contained in said fabricating system, in a plurality of said data bases.

135. A fabricating method according to claim 123, which further comprises the step of controlling the processing and transporting operations by said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters, and the step of managing at least one of said data bases.

136. A fabricating method according to claim 135, wherein said computes distributed in each or a set of said processing apparatuses and said inter-apparatus transporters manage at least one of said data bases on semiconductor wafers contained in each or a set of said

processing apparatuses and said inter-apparatus transporters.

137. A fabricating method according to claim 132, wherein said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters control the processing and transporting operations, and which transmit a data for renewing at least one of said data bases to a computer having a function managing at least one of said data bases.

138. A fabricating method according to claim 137, wherein said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters transmit a data for renewing said data bases, to a computer having a function of managing at least one of data bases containing the managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting on semiconductor wafers contained in each or a set of said processing apparatuses and said inter-apparatus transporters.

139. A fabricating method according to claim 137, wherein said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters receive the managing information of process

progress, scheduling information of processing and transporting or information on result of processing and transporting on semiconductor wafers contained in each or a set of said processing apparatuses and said inter-apparatus transporters, from computers distributed in each or a set of different processing apparatuses and inter-apparatus transporters from each or a set of said processing apparatuses and said inter-apparatus transporters.

140. A fabricating method according to claim 138, wherein when semiconductor wafers in said fabricating system are moved between each or a set of processing apparatuses and inter-apparatus transporters, said managing information of process progress, scheduling information of processing and transporting, or information on result of processing and transporting are moved between said computers by transmission or receiving of managing information of process progress, scheduling information of processing and transporting, or information on result of processing and transporting.

141. A fabricating method according to claim 135, wherein at least two of said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters perform the transmission and

receiving of data by way of the same data field in said fabricating system.

142. A fabricating method according to claim 141, wherein said computers distributed in each or a set of said processing apparatuses and said inter-apparatus transporters transmit a data with a content identification element attached in the data field; and at least one of each or a set of different processing apparatuses and inter-apparatus transporters from each or a set of said processing apparatuses and said inter-apparatus transporters receive a data identified and selected by the content identification element of the data field.

143. A fabricating method according to claim 141, wherein said data field is a memory such as a main line of a local area network, a semiconductor memory or a magnetic disk.

144. A fabricating method according to claim 123, which further comprises the step of generally managing the managing information of process progress and scheduling information of processing and transporting on said semiconductor wafers by computers contained in said fabricating system.

145. A fabricating method according to claim 123, which further comprises the step of generally managing the

information on result of processing and transporting on all of said semiconductor wafers by computers contained in said fabricating system.

146. A fabricating method according to claim 141, wherein said computers having a function of generally managing said information on said semiconductor wafers perform the transmission and receiving by way of the same data field in said fabricating system.

147. A fabricating method according to claim 144, which further comprises the step of generally determining at least part of the operation conditions or scheduling of processing and transporting for all of said semiconductor wafers contained in said fabricating system by said computers having a function of generally managing said information on all of said semiconductor wafers, on the basis of the result of comparing the managing information of process progress and scheduling information of processing and transporting on said semiconductor wafers with each other, or on the basis of the information on result of processing and transporting.

148. A fabricating method according to claim 144, which further the step of applying continued processes to a plurality of semiconductor wafers, on the basis of the scheduling information of processing and transporting

generally managed by said computer having a function of generally managing said information on said semiconductor wafers.

149. A fabricating method according to claim 147, which further comprises the step of applying continued processes to a plurality of semiconductor wafers, on the basis of the scheduling of processing and transporting generally determined by said computer having a function of generally managing said information on said semiconductor wafers.

150. A fabricating system according to claim 141, which further comprises the step of applying continued processes to a plurality of semiconductor wafers, on the basis of the scheduling of processing and transporting generally determined by said computers distributed in each or a set of processing apparatuses and inter-apparatus transporters.

151. A fabricating method according to claim 149, which further comprises the step of providing a plurality of means capable of determining scheduling of processing or transporting in said fabricating system, and displaying which means determine the scheduling of processing and transporting.

152. A fabricating method according to claim 123, which further comprises the step of reading or writing the managing information of process progress, scheduling information of processing and transporting or information on result of processing and transporting which are contained in semiconductor wafers.

153. A fabricating method according to claim 152, which further comprises the step of renewing said information contained in said semiconductor wafers in the processing, transporting or stocking stage.

154. A fabricating method according to claim 152, wherein said semiconductor wafer has the information on result of processing reflected by the result of processing for each semiconductor wafer.

155. A fabricating method according to claim 123, wherein said inter-apparatus transporter is of an inter-apparatus single wafer transporting type, and semiconductor wafers are transported by said inter-apparatus single wafer transporter one by one.

156. A fabricating method according to claim 123, said processing apparatus is of a single wafer processing apparatus, and semiconductor wafers are processed said processing single wafer apparatuses one by one.

157. A fabricating system comprising at least two processing apparatuses and an inter-apparatus transporter for transporting semiconductor wafers to a desired processing apparatus, wherein said inter-apparatus transporter is constituted of partial transporting units, and which has a mechanism for adjusting at least one of positional relationships between said partial transporting units.

158. A fabricating system according to claim 157, wherein said inter-apparatus transporter has a mechanism for adjusting one of positional relationships between partial transporting units without stoppage of the function of the transporting.

159. A fabricating system according to claim 157, wherein a drive force for adjusting at least one of positional relationships between said partial transporting units or between said partial transporting units and processing apparatuses is the gas pressure of air or nitrogen, water pressure, static electric force or magnetic force.

160. A fabricating method according to according to claim 157, which includes a mechanism for monitoring at least one of positional relationships between said partial

transporting units or between said partial transporting units and processing apparatuses.

161. A fabricating method according to claim 160, wherein a laser is used for monitoring at least one of positional relationships between said partial transporting units or between said partial transporting units and processing apparatuses.

162. A fabricating method according to claim 157, wherein at least one of positional relationships between said partial transporting units or between said partial transporting units and processing apparatuses are periodically adjusted.

163. A fabricating system according to claim 157, said inter-apparatus transporter is an inter-apparatus single wafer transporting type.